CLAIM SUMMARY DOCUMENT

1. (Currently Amended) A method of measuring capacitance of micro structures of an integrated circuit, wherein the micro structure has a first terminal and a second terminal separated by an insulator and the integrated circuit includes at least a third terminal separated from the first terminal by an insulator, the method comprising:

applying a biasing ~~voltage~~ potential to the second terminal;

applying ~~the same~~a common potential to the first and third terminals; and

measuring an electrical characteristic between the first and second terminals to determine the capacitance between the first and second terminals.

2. (Currently Amended) The method according to Claim 1, wherein the integrated circuit includes a plurality of third terminals each separated from the first terminal by an insulator; and the method includes applying the ~~same~~ common potential to the first terminal and all of the third terminals.

3. (Currently Amended) The method according to Claim 2, wherein the integrated circuit includes a fourth terminal separated from the first terminal by an insulator; and the method includes applying the biasing ~~voltage~~ potential to the second and fourth terminals, and measuring the electrical characteristic between the first terminal and the second and fourth terminals to determine the sum of the capacitance between the first terminal and the second and fourth terminals.

4. (Currently Amended) The method according to Claim 1, wherein the integrated circuit includes a fourth terminal separated from the first terminal by an insulator; and the method includes applying the biasing ~~voltage~~ potential to the second and fourth terminals, and measuring the electrical characteristic between the first terminal and the second and fourth terminals to determine the sum of the capacitance between the first terminal and the second and fourth terminals.

5. (Currently Amended) The method according to Claim 1, wherein the integrated circuit includes a plurality of fourth terminals separated from the first terminal by insulators; and the method includes applying the biasing ~~voltage~~ potential to the second and

all of the fourth terminals, and measuring the electrical characteristic between the first terminal and the second and all of the fourth terminals to determine the sum of the capacitance between the first terminal and the second and all of the fourth terminals.

6. (Original) The method according to Claim 1, wherein the measurement is taken at the first terminal.

7. (Currently Amended) The method according to Claim 1, wherein the micro structure is a field effect transistor having a gate separated from a source, a drain and a channel area by an insulator; and the capacitance between the gate and the source or drain is measured by:

applying the biasing ~~voltage~~ potential to one of the source or drain connected to the second terminal;

applying the ~~same~~ common potential to the gate, connected to the first terminal, and to the channel area and the other of the source or drain, connected to the third terminal; and

measuring the electrical characteristic between the gate and the one of the source or drain to determine the capacitance between the gate and the one of the source or drain.

8. (Currently Amended) The method according to Claim 7, including:

applying the biasing ~~voltage~~ potential to the source and the drain;

applying the ~~same~~ common potential to the gate and the channel area; and

measuring the electrical characteristic between the gate and the source and drain to determine the sum of the capacitance between the gate and the source and drain.

9. (Currently Amended) The method according to Claim 1, wherein the micro structure is a field effect transistor having a gate separated from a source, a drain and a channel area by an insulator; and the capacitance between the gate and the source or drain is measured by:

applying the biasing ~~voltage~~ potential to the gate connected to the second terminal;

applying the ~~same~~ common potential to one of the source or drain, connected to the first terminal, and to the channel area and the other of the source or drain, connected to the third terminal; and

measuring the electrical characteristic between the gate and the one of the source or drain to determine the capacitance between the gate and the one of the source or drain.

10. (Currently Amended) The method according to Claim 1, wherein the micro structure is a field effect transistor having a gate, and a source and a drain having a PN junction with a body; and the capacitance of the PN junction between one of the source or drain and the body, with a depletion layer resulting there between being the insulator, is measured by:

applying the biasing ~~voltage~~ potential to the body connected to the second terminal;

applying the ~~same~~ common potential to one of the source and drain, connected to the first terminal, and to the gate and the other of the source and the drain, connected to the third terminal; and

measuring the electrical characteristic between the one of the source or drain and the body to determine the capacitance of the PN junction between the one of the source and drain and the body.

11. (Currently Amended) The method according to Claim 1, wherein the integrated circuit includes a memory array of cells, each cell having a) a cell plate, b) a transistor connected to a word line and a bit line and c) a body; and the capacitance between a word or bit line and its neighbor word or bit line respectively is measured by:

applying the biasing ~~voltage~~ potential to the neighbor word or bit line connected to the second terminal;

applying the ~~same~~ common potential to the word or bit line, connected to the first terminal, and to the cell plate and the body, connected to the third terminal; and

measuring the electrical characteristic between the word or bit line and the neighbor word or bit line to determine the capacitance between the word or bit line and its neighbor word or bit line.

12. (Currently Amended) The method according to Claim 11, wherein:

the capacitance between a word or bit line and only one of its two neighbor word or bit line respectively is measured by applying the biasing ~~voltage~~ potential to the one neighbor word or bit line, applying the ~~same~~ common potential to the word or bit line, the other

neighbor word or bit line, the cell plate and the body, and measuring the electrical characteristic between the word or bit line and the one neighbor word or bit line; and

the total capacitance between a word or bit line and both of its two neighbor word or bit lines respectively is measured by applying the biasing ~~voltage~~ potential to both neighbor word or bit lines and applying the ~~same~~ common potential to the word or bit line, the cell plate and the body, and measuring the electrical characteristic between the word or bit line and both neighbor word or bit lines.

13. (Original) The method according to Claim 11, wherein the transistors of the cells are turned off.

14. (Original) The method according to Claim 11, including providing a pad on the integrated circuit connected to the bit or word line as the first terminal and a separate pad for the cell plate and body as the third terminal.

15. (Original) The method according to Claim 14, including providing shield electrodes on the integrated circuit adjacent the pad and connected to the third terminal.

16. (Original) The method according to Claim 15, wherein the shield electrodes and the pad are on the same and different levels of the integrated circuit.

17. (Currently Amended) The method according to Claim 1, wherein the integrated circuit includes a plurality of conductors separated by insulators; and the capacitance between a conductor and one of its neighbor conductors is measured by:

applying the biasing ~~voltage~~ potential to the one neighbor conductor connected to the second terminal;

applying the ~~same~~ common potential to the conductor, connected to the first terminal, and to the other conductors, connected to the third terminal; and

measuring the electrical characteristic between the conductor and the one neighbor conductor to determine the capacitance between the conductor and the one neighbor conductor.

18. (Original) The method according to Claim 17, wherein the conductors are on the same and different levels of the integrated circuit and the conductor and the one conductor can be on the same or different levels of the integrated circuit.

19. (Original) The method according to Claim 17, wherein the conductors are one or more of metal and polycrystalline.

20. (Currently Amended) A method of measuring capacitance of field effect transistor of an integrated circuit, the field effect transistor having a gate, a source, a drain and a channel area; the method comprising:

applying ~~the~~ a biasing ~~voltage~~ potential to one of the gate, source or drain;

applying ~~the same~~(a) a common potential to the gate ~~and to~~, the channel area and the other of the source or drain if the biasing ~~voltage~~ potential is applied to the one of the source or drain, and (b) the ~~same~~ common potential to one of the source or drain ~~and to~~, the other of the source or drain and the channel area if the biasing ~~voltage~~ potential is applied to the gate; and

measuring an electrical characteristic between the gate and the one of the source or drain to determine the capacitance between the gate and the one of the source or drain.

21. (Currently Amended) The method according to Claim 20, wherein the source and the drain each have a PN junction with a body; and the capacitance of the PN junction between one of the source or drain and the body is measured by:

applying the biasing ~~voltage~~ potential to the body;

applying the ~~same~~ common potential to one of the source and drain and to the gate and the other of the source and the drain,; and

measuring the electrical characteristic between the one of the source and drain and the body to determine the capacitance of the PN junction between the one of the source and drain and the body.

22. (Currently Amended) A method of measuring capacitance of an integrated circuit which includes a memory array of cells, each cell having a) a cell plate, b) a transistor

connected to a word line and a bit line and c) a body; and the capacitance between a word or bit line and its neighbor word or bit line respectively is measured by:

applying ~~the~~ a biasing ~~voltage~~ potential to the neighbor word or bit line;

applying ~~the same~~a common potential to the word or bit line and to the cell plate and body; and

measuring an electrical characteristic between the word or bit line and the neighbor word or bit line to determine the capacitance between the word or bit line and the neighbor word or bit line.

23-25. (Canceled)